

ABSTRACT

A method for designing at least one mask for manufacturing an integrated circuit is disclosed. The method may include generating a schematic; entering data representing transistors of the set into a computer-aided design system; identifying transistors expected to be subject to voltage levels beyond the bounds of a power rail and a ground rail; designating robust geometries such transistors and operating the computer-aided design system to generate mask or masks. Integrated circuits of scalable design are also disclosed.